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21. (Amended) A method of manufacturing a semiconductor device for building a circuit composed of combined plural intellectual properties into a semiconductor chip, comprising:

arranging each mask pattern of said plural intellectual properties for a layout pattern.

22. (Amended) The method of manufacturing a semiconductor device according to

Claim 21, wherein

said each mask patterns of said plural intellectual properties has a mark for positioning, and

positioning of said mask patterns is performed by superposing one of said marks on another of said marks.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 21-24 are presently active in this case, Claims 21 and 22 amended by way of the present amendment.

In the outstanding Official Action the title was objected to; Claims 21-24 were rejected under 35 U.S.C. §112, second paragraph; and Claims 21-24 were rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent 3,760,384 to Krolikowski et al.

First, Applicants wish to thank Examiner Pyonin and Supervisory Patent Examiner (Spe) Lebentritt for the November 27, 2001 personal interview at which time the outstanding issues in this case were discussed. During the personal interview, the claims were discussed in relation to the cited reference to Krolikowski et al. No agreement was reached.

With regard to the objection to the title, Applicants have now amended the specification to include the title of the invention suggested by the outstanding Official Action. Therefore the objection to the title is believed to be overcome.

With regard to the rejection under 35 U.S.C. §112, second paragraph, Claim 21 has been amended to correct the noted informalities and, therefore, the rejection under 35 U.S.C. § 112, second paragraph is believed to be overcome. Moreover, Claim 21 has been amended to change “circuit elements” to --intellectual properties--. In this regard, it is noted that “circuit element” is recited in relation to “IP (intellectual property)” in the specification at page 2, line 22 - page 3, line 2, and page 31, line 6 - page 34, line 7. Therefore, this amendment to Claim 21 does not raise an issue of new matter.

Turning now to the merits, in order to expedite issuance of a patent in this case, Claim 21 has been amended to clarify the patentable features of the present invention over the cited reference to Krolikowski et al. Specifically, amended Claim 21 recites a method of manufacturing a semiconductor device for building a circuit composed of combined plural intellectual properties into a semiconductor chip, including arranging each mask pattern of the plural intellectual properties for a layout pattern.

In contrast, Krolikowski et al discloses a method of fabricating a FET memory chip. The method uses separate masks to define and form the different regions of the FET devices. The method uses a conventional masking system wherein a first mask is used to form a first part of the FET devices, and subsequent masks are placed over the area of the first mask to form other parts of the FET devices. For example, as described in column 11, lines 23-45, a mask A is used to form the source and drain regions of the FET, and masks B, C, and D are used to form other areas of the FET such as contact holes and metalization patterns. Because each mask defines a portion of the same FET, the masks must be carefully aligned to maintain a desired spacing. As discussed in the November 27th interview, the alignment

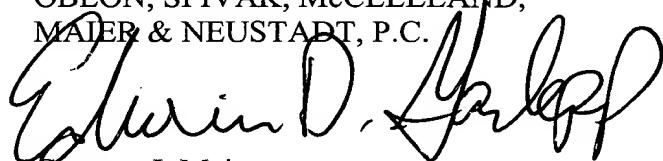
masks of Figure 9 are used to ensure that each mask is placed precisely where the previous mask was placed on the semiconductor chip. Thus, it is Applicant's position that Krolikowski et al does not disclose arranging each mask pattern of said plural intellectual properties for a layout pattern as now recited in Claim 21.

Therefore, Claim 21 patentably defines over the cited reference. Moreover as Claims 22-24 depend from Claim 21, these claims also patentably define over the cited reference.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application and the present application is believed to be in condition for allowance. An early and favorable action is therefore respectfully requested.

Respectfully submitted,

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IN THE SPECIFICATION

Please delete the title of the invention in its entirety and substitute therefor

MANUFACTURING METHOD OF CIRCUIT ELEMENTS ON

A SEMICONDUCTOR WAFER USING A PLURALITY OF MASKS.

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IN THE CLAIMS

Please amend Claims 21 and 22 as follows:

21. (Amended) A method of manufacturing a semiconductor device for building a circuit composed of combined plural [circuit elements] intellectual properties into a semiconductor chip, comprising:

[expressing a layout] arranging each mask pattern of said [circuit by using mask patterns respectively prepared] plural intellectual properties for [said plural circuit elements] a layout pattern.

22. (Amended) The method of manufacturing a semiconductor device according to Claim 21, wherein

[each of] said each mask [pattern] patterns of [respectively prepared for] said plural [circuit elements] intellectual properties has a mark for positioning, and positioning of said mask patterns is performed by superposing one of said marks on another of said marks.